



**B. P. PODDAR INSTITUTE OF MANAGEMENT &  
TECHNOLOGY**  
**DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING**  
**Lesson Plan(PCC-CS-302)**

Lecture No	Topics to be covered	Time	Ref	Teaching Aid
1.	Commonly used number systems. Fixed and floating point representation of numbers.	50	B1,B2	BM
2.	Basic organization of the stored program computer and operation sequence for execution of a program	50	B1	BM
3.	Fetch, decode and execute cycle	50	B1	BM
4.	Concept of operator, operand, registers and storage	50	B1	BM
5.	Instruction format and Instruction sets	50	B1	BM
6.	Addressing modes	50	B1	BM, P.P.T
7.	Addressing modes cont..	50	B1	BM, P.P.T
8.	Role of operating systems and compiler/assembler	50	B1	BM
9.	Floating point - IEEE 754 standard.	50	B1	BM
10.	Multiplication-shift and add	50	B1	BM
11.	Fixed point multiplication -Booth's algorithm	50	B1	BM
12.	Binary adder- serial adder, Ripple carry adder	50	B1	BM
13.	Carry Look-Ahead Adder, Difference between R.C.A & C.L.A	50	B1	BM
14.	Carry Save multiplier	50	B1	BM
15.	Overflow & Underflow concept with examples	50	B1	BM
16.	Fixed point division – Restoring Fixed point division - Restoring	50	B1	BM, P.P.T
17.	Fixed point division – Non Restoring division algorithm	50	B1	BM, P.P.T
18.	Design of ALU.	50	B1	BM, P.P.T
19.	Memory hierarchy, Different memory access parameter	50	B1	BM
20.	Memory organization, static and dynamic memory	50	B1	BM
21.	Memory unit design with special emphasis on implementation of CPU memory interfacing	50	B1	BM, Think-Pair-Share
22.	Construction of large memory using small memory with examples	50	B1,B2	BM
23.	Associative memory, C.A.M, Locality Of Reference	50	B1	BM
24.	Cache memory, Cache mapping techniques with examples	50	B1	BM, P.P.T

25.	Virtual memory, M.M.U	50	B1	BM, P.P.T
26.	Page table, Paging, Segmentation	50	B1	BM
27.	Replacement Policies	50	B1	BM
28.	Mathematical Problems	50	B1,B2, B3	BM
29.	Data path design for read/write access	50	B1	BM
30.	Introduction to parallel processors, Concurrent access to memory and cache coherency.	50	B1	BM
31.	Design of control unit(single bus architecture)	50	B3	BM
32.	Hardwired control Unit	50	B1	BM
33.	Microprogrammed control unit	50	B1	BM
34.	Introduction to pipelining, Instruction pipelining,	50	B3	BM
35.	Pipelining Hazard- classification & solution	50	B3	BM
36.	Introduction to RISC and CISC architectures, RISC vs CISC architectures	50	B1	BM,P.P.T
37.	Introduction to I/O operations	50	B1	BM
38.	Concept of handshaking	50	B1	BM
39.	Polled I/O	50	B1	BM
40.	Interrupt and DMA	50	B1,B3	BM

#### Required Text Books:

**B1.** Ghosh T.K., “Computer Organization and Architecture”, third edition, McGraw Hill

#### Required Reference Books:

**B2.** Mano, M.M, “Computer System Architecture”, second edition, PHI

**B3.** Hayes J.P., “Computer Architecture and Organization”, third edition, McGraw Hill

#### Web references

W1. <https://nptel.ac.in/courses/106103068/pdf/coa.pdf>

W2. <https://www.geeksforgeeks.org/computer-organization-and-architecture-gq>

W3. [guides.lib.monash.edu/c.php?g=219786&p=1454301](https://guides.lib.monash.edu/c.php?g=219786&p=1454301)

#### Required Reference Teaching Aid:

BM- Board & Marker

P.P.T- Power Point presentation

