B. P. Poddar Institute of Management & Technology

Department of Electronics & Communication Engineering

Lesson plan for Digital System Design (EC-302)

Academic Year: 2024-2025

After completion of the course students will be able to-

Module	Hr	Sub-Topic (from syllabus)	Instructional Learning Outcome (ILO) (Cognitive Process /Knowledge Dimension)	Topic Learning Outcome (TLO)	Course Outcome (CO)
I	4	Review of Number System, Signed and Unsigned Number. Logic Simplification and Combinational Logic Design: Review of Boolean Algebra and De Morgan's Theorem, SOP & POS forms, Canonical forms, Karnaugh's map, Binary codes, Code Conversion.	1.1 Comprehensive idea of different number system. (U/CK) (PI-1.3.1,12.2.1) 1.2 Understand the concept of Boolean algebra apply the same for logical simplification. (A/PK) (PI-1.3.1,2.1.2, 12.2.1,) 1.3 Synthesize the SOP and POS canonical form for simplification using Karnaugh's map (A/PK) (PI- 1.3.1, 2,1,2,12.2.1) 1.4 Apply the concept of number system for performing different code conversion. (A/PK) (PI- 1.3.1, 2.1.2,12.2.1)	TLO1: Analyze different number system and understand the concept of Boolean algebra. TLO2: Use K-map for logical simplification and perform different code conversion.	**CO1:** Demonstrate different types of codes, number systems and minimization techniques used in digital system design. (**Apply**) Assessment Tools: QUIZ
I	4	MSI devices like Comparators, Multiplexers, Encoder, Decoder, H-alf and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder, Fast adders, Barrel shifter and ALU.	2.1 Design Comparators, half-adder, full adder, and subtractor. (U/CK) (PI-1.3.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.3,2.4.4,12.2.1,12.2.2) 2.2 Construct the multiplexer, demultiplexer circuit, encoder and decoder circuit. (A/PK) (PI-1.3.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.3,2.4.4,12.2.1,12.2.2) 2.3 Design BCD adder and Fast Adders. (A/PK) (PI-1.3.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.3,2.4.4,12.2.1,12.2.2) 2.4 Design Barrel Shifter and ALU. (Analyse/PK) (PI-1.3.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.3,2.4.4,12.2.1,12.2.2)	TLO1: Appy the circuit concept for various arithmetic operation. TLO2: Apply the circuit concept for implementing different logical function. TLO3: Apply the concepts for developing processing unit of Computational devices.	**CO2:** Design and analyze different combinational logic circuits (**Apply**) Assessment Tools: CT, PS
II	6	Sequential Logic Design: Building blocks like S-R, JK and Master Slave JK FF, Edge triggered FF, Ripple and Synchronous counters, Shift registers, Finite state machines, Design of synchronous FSM.	3.1 Deign different Flip Flop and Develop the Characteristic equation for the same. (U/CK) ((PI-1.3.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.3,2.4.4,12.2.1,12.2.2) 3.2 Design Shift registers Circuits. (A/PK) (PI-1.3.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.3,2.4.4,12.2.1,12.2.2) 3.3 Design ripple and Synchronous Counter (Analise/PK)	TLO1: Apply the concept of Flip flop to design various Synchronous circuit. TLO2: Apply the concept of Flip flop to design various	**CO3:** Design and analyze different sequential logic circuits. (**Apply**) Assessment Tools: CT, TP

		Designing synchronous circuits like Synchronous Counter, Pulse train generator, Pseudo Random Binary Sequence generator,	(PI-1.3.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.3,2.4.4,12.2.1,12.2.2) 3.4 Design Different Finite State machines. (PI-1.3.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.3,2.4.4,12.2.1,12.2.2) 3.5 Design different sequence generator. (PI-1.3.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.3,2.4.4,12.2.1,12.2.2)	Asynchronous circuit.	
III	8	Logic Families and Semiconductor Memories: TTL, ECL, CMOS families Semiconductor Memories, Concept of Programmable logic devices like FPGA. Logic implementation using Programmable Devices. Different types of A/D and D/A conversion techniques. Sample & Hold Circuit	4.1 Describe Different logic families like TTL, ECL, CMOS. (PI-1.3.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.3,2.4.4,4.1.1,4.1.2,12.2.1,12.2.2) 4.2 Understand Different semiconductor memories (U/CK) (PI-1.3.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.3,2.4.4,4.1.1,4.1.2,12.2.1,12.2.2) 4.3 Explain Different type of Analog to digital converter. (A/PK) (PI-1.3.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.3,2.4.4,4.1.1,4.1.2,12.2.1,12.2.2) 4.4 Explain Different type of digital to analog converter. (PI-1.3.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.3,2.4.4,4.1.1,4.1.2,12.2.1,12.2.2)	TLO1: Compare different logic families in terms of different parameters like noise fan-in fan-out, speed of operation power etc., and compare semiconductor memories, different converter for their performances.	**CO4:** Compare different logic families in terms of speed, power consumption, noise etc. and different analog and digital data converters. (Evaluate) Assessment Tools: CT, PS, TP
IV	8	VLSI Design flow: Design entry Schematic, FSM & HDL, different modeling styles in VHDL, Data types and objects, Dataflow, Behavioral and Structural Modeling, Synthesis and Simulation. VHDL constructs and codes for combinational and sequential circuits.	5.1 Explain different Design entry schematics & HDL Data types and objective. (U/CK) (PI-1.3.1,2.1.2,2.1.3,12.2.1) 5.2 Understand different Dataflow modeling, Behavioral and Structural modeling. (A/PK) (PI-1.3.1,2.1.2,2.1.3 ,12.2.1) 5.3 Apply the VHDL modeling for designing the combinational design circuit (A/CK) (PI-1.3.1,1.4.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.4,3.1.1,3.1.6,3.2.1,3.2.3,3.4.1,3.4.2,12.2.1) 5.4 5.4 Apply the VHDL modeling for designing the Sequential design circuit (A/CK) (PI-1.3.1,1.4.1,2.1.2,2.1.3, 2.2.1,2.2.2,2.3.1,2.4.4,3.1.1,3.1.6,3.2.1, 3.2.3,3.4.1,3.4.2,12.2.1)	TLO1: Develop VHDL code for different Digital logic circuit.	**CO5:** Implementation of different logic circuits using programmable device and HDL (**Create**) Assessment Tools: PS, TP

CO-PO mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1										1	2	1
CO2	2	3										2	2	1
CO3	2	3										2	2	1
CO4	2	3		2								2	1	1
CO5	2	2	2									1	1	1
Course	**2**	**2.4**	**0.4**	**0.4**	**0.00**	**0.00**	**0.00**	**0.00**	**0.00**	**0.00**	**0.00**	**1.6**	**1.6**	**1.00**

Summary of sub-topic of COs and POs relation

CO	No. of ILOs	No. of PIs associated with POs	% Of ILOs related with Pos
CO1	4	PO1: 05	PO1- 1 (20%), PO2- 1(7.69%), PO12-1(16.67%)
CO2	4	PO2: 13	PO1- 1 (20%), PO2- 7 (53.85%), PO12-2(33.33%)
CO3	5	PO3: 13	PO1- 1 (20%), PO2- 7(53.85%), PO12-2(33.33%)
CO4	4	PO4:10	PO1- 1 (20%), PO2- 7 (53.85%), PO4-2(20%), PO12-2(33.33%)
CO5	4	PO12: 06	PO1- 2 (40%), PO2- 6 (46.15%), PO3-6(46.15), PO12-1(16.67%)

Rubric for CO PO PSO mapping:

Methods	Attainment Levels	
=PI mapped with CO/PO given	Level 1	<20
	Level 2	>=20 and <50
	Level 3	>=50