B.P. PODDAR INSTITUTE OF MANAGEMENT AND TECHNOLOGY
Department of Computer Science and Engineering
Computer Architecture
PCC-CS402
AY:2024-25

Computer Architecture Code:
PCC-CS402

Contacts: 3L

Name of the Course:	**Computer Architecture**		
CourseCode:PCC-CS402	Semester: IV		
Duration:6 months	Maximum Marks:100		
Teaching Scheme		**Examination Scheme**	
Theory:3hrs./week		MidSemesterexam:15	
Tutorial: NIL		Assignment and Quiz:10marks	
		Attendance: 5 marks	
Practical: hrs./week		EndSemesterExam:70 Marks	
Credit Points:	3		
Faculty Name:	Somali Sikder		
Objective:			
1	To learn the basics of stored program concepts.		
2	To learn the principles of pipelining		
3	To learn mechanism of data storage		
4	To distinguish between the concepts of serial, parallel, pipeline architecture.		
Pre-Requisite:			
1	BasicStructureofComputers,Functionalunits,software,performanceissues software, machine instructions		
2	RAM, ROM, Memory management		

Unit	Content	Hrs/Unit	Marks/Unit

1	Introduction: Review of basic computer architecture (Revisited), Quantitative techniques in computer design, measuring and reporting performance. (3L) Pipelining: Basic concepts, instruction and arithmetic pipeline, data hazards, control hazards and structural hazards, techniques for handling hazards. Exception handling. Pipeline optimization techniques; Compiler techniques for improving performance. (9L)	12	
2	Hierarchical memory technology: Inclusion, Coherence and locality properties; Cache memory organizations, Techniques for reducing cache misses; Virtual memory organization, mapping and management techniques, memory replacement policies. (8L)	8	
3	Instruction-level parallelism: basic concepts, techniques for increasing ILP, superscalar, super-Pipelined and VLIW processor architectures. Array and vector processors. (6L)	6	
4.	Multiprocessor architecture: taxonomy of parallel architectures; Centralized shared- memory architecture: synchronization, memory consistency, interconnection networks. Distributed shared- memory architecture. Cluster computers. (8L) Non von Neumann architectures: data flow computers, reduction computer architectures, systolic architectures. (4L)	7	

COURSE OUTCOMES:

SNO	DESCRIPTION	Cognitive Levels
PCC-CS402.1	**Explain** pipelining concepts using prior knowledge of the stored program method.	Understand(L2)
PCC-CS402.2	**Analyze** memory hierarchy and memory mapping techniques.	Analyze(L4)

PCC-CS402.3	**Describe** parallel architecture and interconnection networks. (Describe taxonomy of parallel architectures. Explain memory consistency models.)	Understand(L2)
PCC-CS402.4	**Compare** ILP processor designs including Superscalar and VLIW.	Analyze(L4)
PCC-CS402.5	**Describe** non-von Neumann architectures such as dataflow and systolic systems.	Understand(L2)

COURSE OUTCOMES VS POs/PSOs MAPPING (DETAILED; HIGH: 3; MEDIUM: 2;

SNO	PO1 (3)	PO2 (4)	PO3 (6)	PO4 (5)	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
PCC-CS402.1	2	2	1	1									1	1
PCC-CS402.2	3	3	2	2				1				1	2	2
PCC-CS402.3	2	2	1	1				1					1	1
PCC-CS402.4	3	3	2	2				1				1	2	2
PCC-CS402.5	2	2	1	1									1	1
CO	5	5	5	5				5					5	5
AVG.	2.4	2.4	1.4	1.4				1				1	1.4	1.4

LOW:1**):**

CO	PO/PSO Mapped	Justification

PCC-CS402.1	PO1-PO4,PSO1,2	PO1: Moderately mapped as engineering knowledge as Students apply prior knowledge of the stored program concept to understand pipelining. PO2: Moderately mapped as they analyze the problem of idle CPU stages and hazards (data, control, structural). PO3: Slightly mapped as they only see how pipelining stages are designed to make CPU execution faster and more efficient. PO4: Slightly mapped as they compare pipelined vs non-pipelined execution using CPI and throughput calculations. PSO1: Slightly mapped as the knowledge gained will aid the students use the stored program concept (fetch–decode–execute cycle) to understand how pipelining overlaps these stages. This shows application of basic computing knowledge in CPU performance improvement. PSO2:
PCC-CS402.2		PO1: Strongly mapped as the Students apply basic knowledge of computer architecture to understand memory hierarchy and mapping. PO2: Strongly mapped as the student analyze the problem of slow memory access and learn how mapping techniques reduce access time. PO3: Moderately mapped as the Students study how to design cache organization (direct/associative/set-associative) for efficient memory usage. PO4: Moderately mapped as the students compare hit ratio, miss ratio, and access time for different mapping techniques. PO8: Slightly mapped as **Ethical use of memory resources for efficient, low-cost, and energy-conscious computing.** PSO1: Moderately mapped as conceptual depth in memory systems to pursue advanced studies, research, and innovations in computer architecture. PSO2: Moderately mapped as it help to develop teamwork and problem-solving skills by applying memory hierarchy concepts for project related work.

PCC-CS402.3		PO1 : Moderately mapped as the Students use basic computer architecture knowledge to understand parallel systems. PO2 : Moderately mapped Students analyze performance issues like latency, bandwidth, and processor communication overhead. PO3 : Slightly mapped as the Students get a basic idea of designing interconnection networks and memory consistency approaches. PO4: Slightly mapped as Students compare different architectures and memory models in terms of efficiency. PO8: Slightly mapped as create Awareness of energy-efficient and sustainable use of parallel systems. PSO1: Slightly mapped as Understanding different parallel architectures and memory models builds a foundation for higher studies and research in advanced areas like distributed computing, AI, and data science. PSO2: Slightly mapped as Teamwork projects often use knowledge of architectures and consistency models .
PCC-CS402.4		PO1: Strongly mapped as the Students use their knowledge of computer architecture to compare Superscalar and VLIW PO2: Strongly mapped as the student Students examine how instruction order, hazards, and scheduling affect performance in Superscalar and VLIW processors. PO3: Moderately mapped as the Students learn how instruction pipelines are structured in ILP processors. PO4: Moderately mapped as Students investigate performance metrics such as IPC, CPI, and throughput in different ILP designs. PO8: Slightly mapped as Students become aware of energy-efficient processor designs for sustainability. PO12: Slightly mapped as students realize processor technology changes fast, so lifelong learning is needed. PSO1: Moderately mapped Useful for higher studies and research in computer architecture and compilers. PSO2: Moderately mapped as Team projects on ILP (scheduling, parallelism) prepare students for industry work.

PCC-CS402.5		PO1: : Moderately mapped as the Students apply their knowledge of computer architecture to understand advanced models like dataflow, reduction, and systolic systems. PO2: : Moderately mapped Students analyze how these architectures differ in execution methods and performance compared to the von Neumann model. PO3 : Slightly mapped as the Students gain basic understanding of design ideas in alternative architectures. PO4: Slightly mapped as students learn advantages such as parallelism, throughput, and speedup. PO8: Slightly mapped as Students get awareness of processors made for low power use and specific tasks. PSO1: Slightly mapped as it Provides background useful for higher studies and research in advanced computing domains. PSO2: Slightly mapped as Students learn teamwork skills while applying these architectures to practical problems.

Lesson Plan:

Paper: Computer Architecture PaperCode:PCC-CS402

L.NO	Topics Covered	Books	Teaching Aids	Teaching Methodology
L1	Introduction to Computer Architecture–Overview	T1,R1	Greenboard	C&T
L2	Quantitative Techniques in Design	T3	Greenboard	C&T
L3	Measuring and Reporting Performance	T4	PPT	C&T
L4	Basics of Pipelining	T4	Greenboard	C&T
L5	Instruction Pipeline	T4	Greenboard	C&T
L6	Arithmetic Pipeline	T4	Greenboard	C&T
L7	Pipeline Hazards–Data Hazards	T2	PPT	C&T

L8	Pipeline Hazards–Control & Structural Hazards	T4	Greenboard	C&T
L9	Exception Handling in Pipelines	T4	Greenboard	C&T
L10	Optimization Techniques in Pipelines	T4	Greenboard	C&T
L11	Compiler Techniques for Pipeline Optimization	T4	PPT	C&T
L12	Revision of Pipelining	T4	Greenboard	C&T
L13	Introduction to Memory Hierarchy	T4	Greenboard	C&T
L14	Inclusion, Coherence, and Locality Principles	T4	PPT	C&T
L15	Cache Memory Organization	T4	Greenboard	C&T
L16	Cache Misses & Reduction Techniques	T4	Greenboard	C&T
L17	Virtual Memory–Concepts and Mapping	T4	Greenboard	C&T
L18	Memory Replacement Policies	T4	Greenboard	C&T
L19	Paging, Segmentation Basics	T4	PPT	C&T
L20	Hierarchical Memory Design–Summary	T4	Greenboard	C&T
L21	Introduction to Instruction-Level Parallelism(ILP)	T4	PPT	C&T
L22	Superscalar Architectures	T4	Greenboard	C&T
L23	Super-Pipelined Architectures	T4	PPT	C&T
L24	Very Long Instruction Word(VLIW)Processors	T4	Greenboard	C&T
L25	Vector Processors	T3	PPT	C&T
L26	Array Processors	T3	PPT	C&T
L27	ILP Techniques–Summary	T4	Greenboard	C&T
L28	Multiprocessor Architecture: Overview	T4	PPT	C&T
L29	Taxonomy of Parallel Architectures	T4	PPT	C&T
L30	Centralized Shared Memory Architecture	T4	PPT	C&T
L31	Synchronization and Memory Consistency	T4	Greenboard	C&T
L32	Interconnection Networks	T4	PPT	C&T

L33	Distributed Shared Memory Architecture	T4	Greenboard	C&T
L34	Cluster Computers	T4	Greenboard	C&T
L35	Non-von Neumann Architectures–Introduction	T4	Greenboard	C&T
L36	Data flow Architectures	T4	Greenboard	C&T
L37	Systolic Architectures	T4	PPT	C&T
L38	Reduction Computers	T4	Greenboard	C&T
L39	Full Syllabus Recap and MCQs	T4,R1	Greenboard	Interactive Q&A
L40	Mock Test and Discussion	T4,R1	Greenboard	Problem Solving

Text Books

T1:V.Carl,G.Zvonko,andS.G.Zaky,*ComputerOrganization*, McGrawHill T2: Barry Brey, C.R. Sarma, *The Intel Microprocessors*, Pearson

T3:J.L.HennessyandD.A.Patterson,*ComputerArchitecture–AQuantitativeApproach*,MorganKaufmann T4: W. Stallings, *Computer Organization*, PHI

Reference Books

R1: Rajaraman, Computer Organization &Architecture, PHI
R2:B.Ram,ComputerOrganization&Architecture,NewAge
R3:Y.C.LieuandG.A.Gibson,MicrocomputerSystems:The8086/8088 Family,PHI R4: J. Uffenbeck, The 8086/8088 Design, Programming, Interfacing, PHI
R5:P.BarryandP.Crowley,ModernEmbeddedComputing,MorganKaufmann

Web References:

W1:NPTEL.ComputerArchitecture.
https://nptel.ac.in/courses/106102062
W2: Geeks for Geeks. Computer Organization and Architecture Tutorials
https://www.geeksforgeeks.org/computer-organization-and-architecture-tutorials

W3:TutorialsPoint.AdvancedComputerArchitecture
https://www.tutorialspoint.com/advanced_computer_architecture/index.htm

CURRICULAR GAP AND MAPPING TO PO/PSO

S.NO	DESCRIPTION	PROPOSED ACTIONS	PO/PSO MAPPED	LEVEL OF MAPPING
1	Parallel Processing	YOUTUBE, NPTEL	PO1,PO5, PO12,PSO 2	3, 2,2,2

WEB SOURCE REFERENCE:

1	https://onlinecourses.nptel.ac.in/noc22_cs47/preview
2	https://onlinecourses.nptel.ac.in/noc21_cs56/preview
3	https://ict.iitk.ac.in/courses/java-a-practical-approach/
4	https://onlinecourses.swayam2.ac.in/aic20_sp13/preview
5	https://www.youtube.com/watch?v=u7eNcAMPVV8

DELIVERY/INSTRUCTIONAL METHODOLOGIES:

CHALK & TALK	STUD. ASSIGNMENT	WEB RESOURCES	NPTEL/OTHERS
LCD/SMART BOARD /PROJECTOR	☐ STUD. SEMINARS	☐ ADD-ON COURSES	☐ WEBNIARS

ASSESSMENT METHODOLOGIES-DIRECT

ASSIGNMENTS	☐ STUD. SEMINARS	TESTS/MODEL EXAMS	UNIV. EXAMINATION
☐ STUD. LAB PRACTICES	☐ STUD. VIVA	☐ MINI/MAJOR PROJECTS	☐CERTIFICATIONS
☐ ADD-ON COURSES	☐ OTHERS		

ASSESSMENT METHODOLOGIES-INDIRECT

ASSESSMENT OF COURSE OUTCOMES (BY FEEDBACK, ONCE)	STUDENT FEEDBACK ON FACULTY
☐ ASSESSMENT OF MINI/MAJOR PROJECTS BY EXT. EXPERTS	☐ OTHERS

Teaching Methods: C&T:-Chalk & Talk; S/P:-Slides/PPT; Videos; SEM: Seminar; DEMO; CHART; ET/GL: Expert Talk/Guest Lecture; QUIZ; GD:-Group discussion; RTCS: Real time

case studies; JAR:-Journal article review; PD:-Poster design; OL:-Online lecture/Google class room

Periodic Monitoring:

Course Activity		Review1		Review2	
		From	To	From	To
		Feb'25	Mar'25	April'25	May'25
Syllabus covered(%)					
Lectures	**Planned(No.)**	**18**		**20**	
	Taken(No.)	**15**		**17**	
Tutorials/Remedial Class	**Planned(No.)**	**1**		**1**	
	Taken(No.)	**1**		**1**	
Assignments	**Planned(No.)**	**01**		**01**	
	Taken(No.)	**01**		**01**	
CA1,CA2	**Planned Dates**	17/02/2025	20/02/2025	4/05/2025	10/05/2025
	Taken Dates				
CA3,CA4	**Planned Dates**	25/03/2025	29/03/2025	5.05.2025	10.05.23
	Taken Dates				
Specify any other (Guest lecture, Workshop, Seminar etc. as mentioned in Lesson Plan)	**Planned Dates**	-	-	-	-
	Taken Dates	-	-	-	-
Signature of Faculty		SOMALI SIKDER (SANYAL)			
Signature of Programme Coordinator					
Signature of HOD					