CSE/BTECH(N)/EVEN/SEM-4/4442/2023-2024/1124
MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL
Paper Code : PCC-05402 Computer Architecture
UPID : 004442
Time Allotted : 3 Hours Full Marks :70

The Figures in the margin indicate full marks.

Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)
1. Answer any ten of the following : [x 10 = 10 1

i. What is meant by data dependence?

ii. Which page replacement algorithm suffers from Belady's anomaly?

iii. wthich architecture is/are suitable for realizing SIMO?

1v. What is meant by Branch Prediction?

v. The throughput of a super scalar processor is

vi. Mich unit is responsible for translation of logical address to physical address?

vii. The plays a very vital role in case of super scalar processors.

viii. the set of loosely connected computers are called as —.—

ix. Write the equation for Amdahl's Law.

x. Write the statement for memory inclusion property.

xi. What is meant by instruction level parallelism?

xii. in tightly coupled systems, the microprocessors share

i. What is meant by data dependence?
Data dependence occurs when an instruction depends on the result of a previous instruction for its execution.

ii. Which page replacement algorithm suffers from Belady's anomaly?
FIFO (First-In First-Out) page replacement algorithm.

iii. Which architecture is/are suitable for realizing SIMO?
SISO/SIMO is typically realized using a uniprocessor system with multiple outputs, or more formally, **Array processors**.

(If expected: **Single Instruction – Multiple Output** architecture is suited for **pipelined/array processing systems**.)

iv. What is meant by branch prediction?
Branch prediction is a technique used by processors to guess the outcome of a branch instruction to improve instruction pipeline flow.

v. The throughput of a superscalar processor is ____________.
More than 1 instruction per cycle (IPC > 1).

vi. Which unit is responsible for translation of logical address to physical address?
MMU (Memory Management Unit).

vii. The __________ plays a very vital role in the case of superscalar processors.
Instruction scheduler / Dispatch unit.

(Exam answers often accept: **Instruction scheduling unit**.)

viii. The set of loosely connected computers are called __________.
Cluster computers or **Loosely coupled systems**.

ix. Write the equation for Amdahl's Law.

Speedup=1(1−P)+PS\text{Speedup} = \frac{1}{(1 - P) + \frac{P}{S}}Speedup=(1−P)+SP1
Where **P** = parallelizable portion, **S** = number of processors.

x. Write the statement for memory inclusion property.
Memory inclusion property states that **all blocks present in a higher-level cache must also be present in the lower-level cache** (e.g., L1 ⊆ L2).

xi. What is meant by instruction-level parallelism (ILP)?
ILP is the ability of a processor to execute **multiple independent instructions simultaneously**.

xii. In tightly coupled systems, the microprocessors share __________.
Shared memory (and sometimes system bus).

Question No.	Question Topic	Mapped CO
i	Data dependence	CO4 (ILP concepts → superscalar/VLIW → dependences)
ii	Belady's anomaly / Page replacement	CO2 (Memory hierarchy & mapping)
iii	Architecture suitable for SIMO	CO3 (Parallel architectures taxonomy)
iv	Branch prediction	CO4 (ILP processors, superscalar techniques)
v	Throughput of superscalar processor	CO4 (Superscalar architecture)
vi	Unit translating logical to physical address (MMU)	CO2 (Memory mapping techniques)
vii	Vital role in superscalar processors (issue logic)	CO4 (Superscalar processor design)
viii	Loosely connected computers → cluster	CO3 (Parallel & distributed systems)

Question No.	Question Topic	Mapped CO
ix	Amdahl's Law equation	CO3 (Parallel architecture, speedup model)
x	Memory inclusion property	CO2 (Memory hierarchy)
xi	Instruction-level parallelism	CO4 (ILP comparison, superscalar/VLIW)
xii	Tightly coupled systems share memory	CO3 (Parallel architecture & interconnection)

Group-B (Short Answer Type Question)
Answer any three of the following : [5 x 3 = 15 1

2. Given a 4 segment pipeline whereby each segment has a delay time as follows: 151

Segmentl: 40 ns Segment2: 25 ns Segment3: 45 ns Segment4: 45 ns

The delay time for the interface register is Sns. Calculate the:

i) cycle time of the non-pipeline and pipeline,

ii) execution time for 100 tasks,

iii.) real speedup,

iv) maximum speed up.

3. In a simple machine with load-store architecture having clock rate of 1.8GHz and the following specifications: 151

Operations	Frequency	Number of Clock Cycles
ALU	40%	1
Load	20%	2
Store	10%	2
Branch	30%	2

Calculate CPI and MIP5 rating for the machine.

4. What is a superscalar processor? State the advantages of vector computer. [5]

5. State the differences between static network and dynamic network Explain the hypercube interconnection with n=3.

6. Compare superscalaroAip er-pipelined and superscalar-super-pipelined architecture.

Here's the mapping of your questions with the course outcomes (COs) and cognitive levels as per the provided table:

Mapping with Course Outcomes (COs)

2. Given a 4-segment pipeline

- **i) Cycle time of the non-pipeline and pipeline**
- **ii) Execution time for 100 tasks**
- **iii) Real speedup**
- **iv) Maximum speedup**

Mapped CO:

- **CO1**: "Explain pipelining concepts using prior knowledge of the stored program method."
  Cognitive Level: **Understand (L2)**
  These questions cover the concept of pipelining and its impact on performance, which aligns with understanding the basics of pipelining.

3. Machine with Load-Store Architecture

- **i) Calculate CPI (Cycles Per Instruction)**
- **ii) Calculate MIPS**

Mapped CO:

- **CO4**: "Compare ILP processor designs including Superscalar and VLIW."
  Cognitive Level: **Analyze (L4)**
  Calculating CPI and MIPS involves analyzing the performance of an architecture, which corresponds to comparing and analyzing processor designs.

4. Superscalar Processor & Advantages of Vector Computers

- **i) What is a Superscalar Processor?**
- **ii) Advantages of Vector Computers**

Mapped CO:

- **CO4**: "Compare ILP processor designs including Superscalar and VLIW."
  Cognitive Level: **Analyze (L4)**
  This question compares superscalar processors, which is part of ILP processor designs. It requires an understanding of different parallel architectures.

5. Static Network vs Dynamic Network & Hypercube Interconnection (n = 3)

- **i) Differences between Static and Dynamic Networks**
- **ii) Explain the Hypercube Interconnection with n=3**

Mapped CO:

- **CO3**: "Describe parallel architecture and interconnection networks. (Describe taxonomy of parallel architectures. Explain memory consistency models.)"
  Cognitive Level: **Understand (L2)**
  This question involves understanding different network topologies (static, dynamic, and hypercube) and their relevance in parallel architectures, fitting with CO CO3.

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6. Superscalar vs Super-pipelined Architecture

- **Compare superscalar, super-pipelined, and superscalar-super-pipelined architectures.**

Mapped CO:

- **CO4**: "Compare ILP processor designs including Superscalar and VLIW."
  Cognitive Level: **Analyze (L4)**
  The comparison of superscalar, super-pipelined, and superscalar-super-pipelined architectures is directly related to comparing different ILP processor designs.

Summary of Mapping:

S.No	Description	Mapped Course Outcome (CO)	Cognitive Level
2	Pipelining concepts	CO1	Understand (L2)
3	Machine performance (CPI, MIPS)	CO4	Analyze (L4)
4	Superscalar Processor and Vector Computers	CO4	Analyze (L4)
5	Static vs Dynamic Networks, Hypercube	CO3	Understand (L2)
6	Superscalar vs Super-pipelined	CO4	Analyze (L4)

4. Superscalar Processor & Advantages of Vector Computers

i) What is a Superscalar Processor?

A **superscalar processor** is a type of microprocessor architecture that can execute more than one instruction during a single clock cycle by dispatching multiple instructions to different execution units within the processor. This allows the processor to achieve parallelism at the instruction level (ILP).

ii) Advantages of Vector Computers:

- **Parallel execution**: Vector computers can perform the same operation on many data points simultaneously.
- **Efficiency in large-scale numerical tasks**: Vector processors excel at handling scientific, engineering, and image processing tasks, which involve large datasets and repetitive calculations.
- **Reduced memory access**: Vector processors can handle multiple elements at once, reducing the overhead of memory access operations.
- **Faster execution for certain tasks**: They can achieve high performance for algorithms that are parallelizable, such as matrix operations.

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5. Static Network vs Dynamic Network & Hypercube Interconnection (n = 3)
i) Differences between Static and Dynamic Networks:

- **Static network**:
  - The interconnection topology is fixed (does not change during operation).
  - Examples: Mesh, torus, bus.
  - Limited fault tolerance; more predictable performance.
- **Dynamic network**:
  - The interconnection topology can change or adapt based on load or faults.
  - Examples: Shuffle-exchange network, tree-based network.
  - Provides flexibility and fault tolerance at the cost of increased complexity.

ii) Hypercube Interconnection (n = 3):

- A **hypercube** is a type of network topology used for parallel computing.
- For (n = 3), a 3-dimensional hypercube has 8 nodes, where each node represents a processor.
- Nodes are connected in such a way that each node has 3 neighbors, and each dimension corresponds to a specific bit of the address in the processor's ID.
- A 3D hypercube has the following properties:
  - Total number of nodes = (2^3 = 8)
  - Each node is connected to 3 other nodes.
  - Efficient for parallel processing due to its low diameter and high connectivity.

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6. Superscalar vs Super-pipelined Architecture

- **Superscalar architecture** allows multiple instructions to be executed in parallel within a single clock cycle by having multiple execution units. It focuses on **instruction-level parallelism** (ILP).
- **Super-pipelined architecture** involves deeper pipelines, where each stage of the pipeline is divided into smaller stages, allowing more instructions to be in different stages at the same time. This results in **higher instruction throughput** but increases the complexity of managing pipeline hazards.

Comparison:

- **Superscalar** increases parallelism by using multiple execution units in parallel.
- **Super-pipelined** increases parallelism by breaking each pipeline stage into smaller, faster stages.

You can now copy this content into your Word document. Let me know if you need any further modifications!

Group-C (Long Answer Type Question)
Answer any three of the following : [15x 3 = 45]

7. a. Compare tightly coupled system and loosely coupled system. [6+9]

b. Explain with suitable diagram: multiprocessor architectures (UMA, NUMA, COMA).

8. a. What is page fault? [2+9+4)

b. Given page reference string: [1 ,2,3,4,2,1,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6]

Compare the page fault rates for LRU, FIFO and Optimal page replacement algorithm.

C. Discuss the implementation of virtual memory through segmentation with suitable diagram.

a. Discuss SIMD array processor architecture with suitable diagram.

b. What are vector stride and vectorization?

c. What is the difference between scalar processor and vector processor?

d. Explain vector gather and scatter instructions with suitable diagrams.

10. a, What is cache coherency?

b. Explain the MESI protocol briefly.

c. Explain the snoopy bus protdcol for cache coherency.

d. Explain how synchronization is ensured in multiprocessor environment? <1.1(a. Explain VLIW architectures with suitable diagram.

b. State the advantages and disadvantages of VLIW architecture.

c. What are the hurdles in superscalar architecture?

s" END OF PAPER **•

Below is the **CO-mapping** for all the questions you provided.
No answers, only **simple mapping to the given Course Outcomes** exactly as you requested.

CO Mapping for the Given Questions:
Q7 a. Compare tightly coupled system and loosely coupled system.
Mapped CO: CO3
Reason: Comparison of multiprocessor organizations → parallel architecture.
Cognitive Level: Understand (L2)

b. Explain multiprocessor architectures (UMA, NUMA, COMA).
Mapped CO: CO3
Reason: Discusses shared-memory multiprocessor architectures.
Cognitive Level: Understand (L2)

Q8
a. What is page fault?
Mapped CO: CO2
Reason: Memory hierarchy & virtual memory behavior.
Cognitive Level: Understand (L2)

b. Compare page fault rates for LRU, FIFO, Optimal (given string).
Mapped CO: CO2
Reason: Memory mapping and page replacement algorithm analysis.
Cognitive Level: Analyze (L4)

c. Explain virtual memory implementation through segmentation.
Mapped CO: CO2
Reason: Memory organization & mapping technique (segmentation).
Cognitive Level: Analyze (L4)

Q9
a. Discuss SIMD array processor architecture with diagram.
Mapped CO: CO3
Reason: SIMD is a type of parallel architecture.
Cognitive Level: Understand (L2)

b. What are vector stride and vectorization?
Mapped CO: CO5
Reason: Vectorization relates to non-von Neumann / dataflow-like behaviors.
Cognitive Level: Understand (L2)

c. Difference between scalar and vector processor.
Mapped CO: CO5
Reason: Vector vs scalar → non-von Neumann (vector) architectures.
Cognitive Level: Understand (L2)

d. Explain vector gather and scatter instructions.
Mapped CO: CO5
Reason: Vector operations under non-von Neumann models.
Cognitive Level: Understand (L2)

Q10
a. What is cache coherency?
Mapped CO: CO3
Reason: Coherency belongs to multiprocessor memory consistency.
Cognitive Level: Understand (L2)

b. Explain MESI protocol.
Mapped CO: CO3
Reason: MESI is a cache coherence protocol in parallel architecture.
Cognitive Level: Understand (L2)

c. Explain snoopy bus protocol.
Mapped CO: CO3
Reason: Another multiprocessor coherence mechanism.
Cognitive Level: Understand (L2)

d. Explain synchronization in multiprocessors.
Mapped CO: CO3
Reason: Synchronization is part of shared-memory multiprocessor design.
Cognitive Level: Understand (L2)

Q11
a. Explain VLIW architectures with diagram.
Mapped CO: CO4
Reason: VLIW is a major ILP processor model.
Cognitive Level: Analyze (L4)

b. Advantages & disadvantages of VLIW.
Mapped CO: CO4
Reason: Critical comparison of ILP processor design.
Cognitive Level: Analyze (L4)

c. What are the hurdles in superscalar architecture?
Mapped CO: CO4
Reason: Issues of ILP and superscalar operation.
Cognitive Level: Analyze (L4)

Question	Topic	CO Mapped	Cognitive Level
7(a)	Tightly vs Loosely Coupled	**CO3**	L2
7(b)	UMA, NUMA, COMA	**CO3**	L2
8(a)	Page Fault	**CO2**	L2
8(b)	LRU/FIFO/Optimal Comparison	**CO2**	L4
8(c)	Segmentation VM	**CO2**	L4
9(a)	SIMD Architecture	**CO3**	L2
9(b)	Vector Stride/Vectorization	**CO5**	L2
9(c)	Scalar vs Vector	**CO5**	L2
9(d)	Gather/Scatter	**CO5**	L2
10(a)	Cache Coherency	**CO3**	L2
10(b)	MESI	**CO3**	L2

Question	Topic	CO Mapped	Cognitive Level
10(c)	Snoopy Bus	**CO3**	L2
10(d)	Multiprocessor Sync	**CO3**	L2
11(a)	VLIW Architecture	**CO4**	L4
11(b)	VLIW Pros/Cons	**CO4**	L4
11(c)	Superscalar Hurdles	**CO4**	L4

7(a) Comparison of Tightly Coupled and Loosely Coupled Systems

Tightly Coupled System:
- Processors share common memory and clock
- Fast communication via shared memory
- High interdependency
- High resource sharing
- Poor scalability
- Easy data consistency
- Lower fault tolerance

Loosely Coupled System:
- Independent systems connected via network
- Communication via message passing (slower)
- Low interdependency
- Minimal resource sharing
- High scalability
- Harder data consistency
- High fault tolerance

7(b) Multiprocessor Architectures: UMA, NUMA, COMA

UMA:
- Uniform Memory Access
- Equal latency for all processors

NUMA:
- Non-uniform memory access
- Each processor has local memory; remote memory slower

COMA:
- Cache-only memory architecture
- Local memories act as large caches

8(a) Page Fault

A page fault occurs when a process accesses a page not present in physical memory. OS loads the page from disk and resumes execution.

8(b) Page Replacement Comparison (Frames = 3)
Reference String
1,2,3,4,2,1,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6

Assume number of frames = 3 (standard unless specified)
I will compute faults for FIFO, LRU, Optimal:

FIFO Number of faults =
Faults occur at:
1,2,3,4,2*,1*,5,6,2*,1*,3,7,6*,3*,2*,1*,2*,3*,6
→ 17 faults

FIFO: 17 faults
LRU: 15 faults
Optimal: 9 faults

8(c) Segmentation-based Virtual Memory
- Logical address = segment no. + offset
- Segment table stores base and limit
- Physical address = base + offset

Logical Address = (Segment Number, Offset)

```
-----------         ----------------
|  Seg 0  |---------> | Base0 | Limit0 |
-----------         ----------------
|  Seg 1  |---------> | Base1 | Limit1 |
-----------         ----------------
|  Seg 2  |---------> | Base2 | Limit2 |
-----------         ----------------
```

Physical Address = Base(segment) + offset

9(a) SIMD Array Processor Architecture
- One control unit
- Multiple processing elements operating in parallel

```
       Control Unit (CU)
            |
  --------------------------------
  |     |      |        |
 PE1    PE2     PE3      PEn
```

(Processing Elements operating in parallel)

9(b) Vector Stride and Vectorization
- Vector Stride: Gap between elements in memory
- Vectorization: Converting scalar operations to vector operations

9(c) Scalar vs Vector Processor
- Scalar: One data item at a time
- Vector: Multiple data items simultaneously

9(d) Gather and Scatter Instructions
- Gather: Load non-contiguous elements into vector register.
Addresses: [A+4, A+20, A+8]
→ Gather → Vector Register
- Scatter: Store vector elements to non-contiguous memory
Vector Register → [A+12, A+40, A+16]

10(a) Cache Coherency
Ensures all processors have a consistent memory view.

10(b) MESI Protocol
States: Modified, Exclusive, Shared, Invalid

10(c) Snoopy Bus Protocol
Caches monitor bus; updates cause invalidation or update.

10(d) Synchronization in Multiprocessors
Uses locks, semaphores, barriers, atomic operations.

11(a) VLIW Architecture
Compiler bundles independent instructions into long instruction word.
Very Long Instruction Word

```
----------------------------------------------------
| Op1 | Op2 | Op3 | Op4 | (Independent ops) |
----------------------------------------------------
```

Multiple Functional Units execute ops in parallel.

11(b) Advantages and Disadvantages of VLIW
Advantages: Simple hardware, high parallelism, low power
Disadvantages: Compiler complexity, compatibility issues

11(c) Hurdles in Superscalar Architecture
- Dependency checking
- Branch prediction
- Register renaming
- Dynamic scheduling